

# Intuitive CMOS Electronics

---

The Revolution in VLSI, Processing,  
Packaging, and Design

*Revised Edition*

Thomas M. Frederiksen



McGraw-Hill Publishing Company

New York St. Louis San Francisco Auckland  
Bogotá Hamburg London Madrid Mexico  
Milan Montreal New Delhi Panama  
Paris São Paulo Singapore  
Sydney Tokyo Toronto

---

Intuitive  
CMOS  
Electronics

## McGraw-Hill Series in Intuitive IC Electronics

---

*This series will help the reader gain an intuitive understanding of electronics and computers. Mathematics is kept to a minimum, as the reader gets "inside" the devices and circuits to grasp, from the electron level up, the workings of integrated circuits, digital computers, operational amplifiers, and other electronics-related topics. The following volumes are planned for the series, and each one is written by Thomas M. Frederiksen, whose Intuitive IC Electronics (McGraw-Hill, 1982) has proved popular with engineers, managers, students, and hobbyists worldwide.*

INTUITIVE DIGITAL COMPUTER BASICS: An Introduction to the Digital World (1988)

INTUITIVE ANALOG ELECTRONICS: From Electron to Op Amp (1988)

INTUITIVE OPERATIONAL AMPLIFIERS: From Basics to Useful Applications (1988)

INTUITIVE CMOS ELECTRONICS: The Revolution in VLSI, Processing, Packaging, and Design (1989)

INTUITIVE IC ELECTRONICS, Second Edition (1989)

*For more information about other McGraw-Hill materials, call 1-800-2-MCGRAW in the United States. In other countries, call your nearest McGraw-Hill office.*

# Intuitive CMOS Electronics

---

The Revolution in VLSI, Processing,  
Packaging, and Design

*Revised Edition*

Thomas M. Frederiksen  
†



McGraw-Hill Publishing Company

New York St. Louis San Francisco Auckland  
Bogotá Hamburg London Madrid Mexico  
Milan Montreal New Delhi Panama  
Paris São Paulo Singapore  
Sydney Tokyo Toronto

Library of Congress Cataloging-in-Publication Data

Frederiksen, Thomas M.

Intuitive CMOS electronics.

Rev. ed. of: Intuitive IC CMOS evolution. c1984.

Bibliography: p.

Includes index.

1. Integrated circuits—Very large scale integration.

2. Metal oxide semiconductors, Complementary.

I. Frederiksen, Thomas M. Intuitive IC CMOS evolution.

II. Title.

TK7874.F678 1989 621.381'73 88-22999

ISBN 0-07-021970-2

ISBN 0-07-021971-0 (pbk.)

Copyright © 1989 by McGraw-Hill, Inc. All rights reserved.  
Printed in the United States of America. Except as permitted  
under the United States Copyright Act of 1976, no part of this  
publication may be reproduced or distributed in any form or by  
any means, or stored in a data base or retrieval system, without  
the prior written permission of the publisher.

1234567890 DOC/DOC 8921098

ISBN 0-07-021970-2

ISBN 0-07-021971-0 {PBK.}

The editors for this book were Daniel A. Gonneau and Nancy Young,  
the designer was Naomi Auerbach, and the production supervisor was  
Suzanne W. Babeuf. It was set in Century Schoolbook.

Printed and Bound by R. R. Donnelley & Sons Company

Information contained in this work has been obtained by McGraw-Hill Inc. from sources believed to be reliable. However, neither McGraw-Hill nor its authors guarantees the accuracy or completeness of any information published herein and neither McGraw-Hill nor its authors shall be responsible for any errors, omissions or damages arising out of use of this information. This work is published with the understanding that McGraw-Hill and its authors are supplying information but are not attempting to render engineering or other professional services. If such services are required, the assistance of an appropriate professional should be sought.

For more information about other McGraw-Hill materials,  
call 1-800-2-MCGRAW in the United States. In other  
countries, call your nearest McGraw Hill office.

*This book is dedicated to the many system engineers who, during a nationwide seminar series in 1982, found my 30-minute presentation titled "A Quick Look at the Evolution of IC Processes," interesting.*



# Contents

---

Foreword	xi
Preface to the Revised Edition	xiii
Preface to the First Edition	xv
Acknowledgments	xvii
<b>1 Background on Solid-State Electronics</b>	<b>1</b>
1.1 The Significance of an Amplifying Device	1
Ways to Provide a Source of Electrons	2
Obtaining High Values of Transconductance	4
1.2 A Short History of Amplifying Devices, Logic Circuits, and Linear Circuits	5
Vacuum Tubes	5
Germanium Transistors	5
Silicon Transistors and the Evolution of Logic Circuits	7
The Linear IC Problems	17
The Evolution of Silicon Wafers	20
Bipolar Enhancements	22
<b>2 The Move to MOS</b>	<b>37</b>
2.1 Comparing Transistor Performance—MOS versus Bipolar	37
Effects of Layout Geometry on Performance	41
Transconductance	42
Frequency Response	44
Output Impedance	45
Modeling Accuracy	45
Temperature Effects	46
High Power Limits	46
2.2 PMOS, The First LSI	47
Solving the Early Reliability Problems	49
Basic PMOS Logic Circuits	49
The Benefits of a Depletion Load	50
Poly and the Self-Aligned Silicon Gate	51
2.3 NMOS for Higher Speed	52
Using a Substrate Bias	52
Logic Circuit Benefits	53
Problems in Realizing Linear Circuits	53
2.4 The Birth of CMOS	53
Logic with No DC Power Drain	53
The Early Metal Gate CMOS Process	55
Transmission Gate Logic	56
Static RAMs that Can Be Put to Sleep	58
Benefits and Problems Because of the Extra Devices	58

A Useful Zener Diode Exists in CMOS	62
N-Wells Versus P-Wells in CMOS	62
CMOS is a Natural for Linear Circuits	63
Bulk CMOS and Silicon on Insulators	65
2.5 The NMOS Revolution	66
The Greed for Speed	66
Benefits of Device Scaling for Digital Circuits	68
<b>3 Advances in Wafer Processing</b>	<b>71</b>
3.1 Ion Implanters Replace Diffusion Furnaces	71
3.2 Buried Dielectric Layers Reduce Stray Capacitance	73
3.3 Resists	73
3.4 The Move to Dry Etching Techniques	75
3.5 Thin Film Deposition	79
3.6 Progress in High Resolution Lithography	81
Problems with the Mask Plate Material	82
A Look at Wafer Imaging Techniques	83
E-Beam Exposure Systems	85
X-Ray Lithography	85
Ion-Beam Lithography	86
Control of Contamination	86
3.7 Solving the Interconnect Problem	88
Multi-Layers	88
Effects on Propagation Delay	89
Problems with Pure Metals	90
Polysilicon and Polycides	91
Connecting to the Outside World	93
<b>4 The Present CMOS VLSI Revolution</b>	<b>95</b>
4.1 From Components to Systems	96
4.2 Specifying the New Chips	96
4.3 The Effects on the System Designers	97
4.4 The Effects on the Electronic Companies	97
4.5 The Effects on the Semiconductor Companies	97
4.6 Computer Aids for VLSI Design	98
Cell and Functional-Block Libraries	99
Mask Design	100
4.7 Problems in Checking the Mask Design	100
4.8 The Increasingly Complex Testing Problem	101
<b>5 Standard Circuits in the New CMOS Era</b>	<b>105</b>
5.1 CMOS Linear Circuits	105
Progress in CMOS Op Amps	106
Switched-Capacitor Filters	111
Digital-to-Analog Converters	115
Analog-to-Digital Converters	118
5.2 A High Performance CMOS Logic Family	124
The Process Used	125
The Performance Obtained	125
Electrostatic Discharge Improvement	129
Improving SCR Immunity	130

5.3	Special CMOS Circuits for the New Telephone Systems	130
	Benefits of Digitized-Voice Transmission	131
	The Telecom Problem	132
	Coding and Decoding	132
5.4	CMOS Microprocessors and Memory Products	133
5.5	Die Coatings for Improved Product Reliability	134
5.6	A Multiple-Layer-Metal CMOS Process	134
<b>6</b>	<b>Semicustom and Custom Circuits</b>	<b>147</b>
6.1	CMOS Gate Arrays, Semicustom ICs	147
	The Philosophy and Uses for Gate Arrays	148
	Processes and Performance	149
	Computer-Based Design Aids	154
	Future Possibilities of Gate Arrays	157
6.2	Custom Circuit Alternatives	158
	Standard-Cell Arrays	159
	Functional Block Arrays	160
	Silicon Compilers	160
<b>7</b>	<b>IC Packaging Developments</b>	<b>163</b>
7.1	High-Density Replacements for the Standard Plastic DIP	165
7.2	Pin Grid Array Packages	167
7.3	Tape Automatic Bonding and Tape-Pak	168
<b>8</b>	<b>A Look into the Future</b>	<b>171</b>
8.1	Developing the Single-Chip VLSI Systems of the Future	171
	The Motivation	172
	The New System Architectures	172
8.2	The Silicon Foundry	174
8.3	Software in the VLSI Era	175
8.4	The Limits of Device Scaling	176
8.5	Gallium Arsenide ICs	176
	<b>Bibliography</b>	<b>179</b>
	<b>Index</b>	<b>181</b>



# Foreword

---

The times when information is most valuable are during change or transition to support decision making where the facts are not clear. This book fills that need at one of the most significant transitions in semiconductor technology since the change from germanium to silicon.

Since their introduction, integrated circuits have continuously increased in density because of the significant improvements in photolithography, the reduction in defect densities, and the development of new circuit topologies. It has been a period of rapid advancement in the performance and integration of the products built with semiconductors. Without a dramatic change, however, that progress might have been limited by power density. That is, the integrated circuit density would be limited by the power that the package could effectively remove—not circuit complexity.

Fortunately, technology in the form of silicon gate oxide isolated CMOS has been developed just in time to allow the improvements in density to continue.

This book is about that transition, what it means and how it's taking place. It chronicles an industry during dramatic change and provides a clear explanation of the past, the present, and the implications for the future.

It can be a vital aid to engineers and industry observers who need to plan for the future before it arrives or for anyone who needs to stay abreast of the semiconductor industry move to CMOS.

Mark Levi  
Formerly Director of CMOS Marketing  
National Semiconductor Corp.  
Santa Clara, California



## Preface to the Revised Edition

This revised edition has incorporated much new material, and also many changes and additions were made in the sections on the capabilities and limitations of silicon wafer processing. The semiconductor industry remains very dynamic, and processing innovations are occurring very rapidly. It is impossible for any book to keep up to date with this rapid rate of change, but if the basic ideas associated with processing are understood, along with some of the technology reported by the researchers, the reader will be in a position to more rapidly understand the continuing evolution that takes place in the production lines.

An introduction to "band-gap" voltage references and how the difference between the base-emitter voltages of two matched transistors, the  $\Delta V_{BE}$  voltage, is used to provide a zero temperature coefficient reference voltage has been added as background for a new CMOS op amp that has been included.

A section on Dynamic Safe Area Protection has been included because this novel technique has allowed the output power capability of ICs to be extended to 150 watts. In addition, the incorporation of large-area DMOS power transistors in power MOS ICs is also mentioned.

The story of the search for a good PNP by the IC designers has been added and the recent "vertically integrated PNP" process is described. Although many processing steps are added, this is still reported to be lower cost than dielectric isolation, a competing technology that also provides a good, compatible PNP.

A recent discovery of a way to provide an adjustable resistor, the "trimistor," by making use of the same physical mechanisms that take place in the "zener zapping" trim technology has been included. The group of engineers who worked on this project received the "Best Paper Award" at the 1987 Solid-State Circuits Conference. The physical mechanisms of this new trimistor are described and the way it was incorporated as an in-package adjustable resistor that allowed the benefits of JFET transistors in front of a bipolar op amp, without having to suffer from a large offset voltage, is covered.

The latest in high performance, CMOS op amps, has been added. A new combination of both circuit design innovations and novel device structures (including the clever use of a parasitic lateral NPN bipolar transistor in a  $\Delta V_{BE}$  biasing circuit) allows these op amps to be fabricated with a standard digital CMOS process to insure compatibility with digital circuits. This eases the problem of mixing digital circuitry with high performance linear circuitry on the same chip. A novel "checkerboard-interconnected hexadecimal" (16 individual P-channel transistors), is used to provide two groups of eight paralleled transistors, each of which is used for the pair of differential input transistors of the op amp. This trick, plus

careful circuit design, essentially solves the usual problem of high offset voltage in CMOS op amps. These general purpose op amps challenge the old position of supremacy that bipolar op amps have long held.

It is my hope that this book continues to provide a good intuitive introduction to wafer processing and also the background that is needed to more fully appreciate the VLSI era, and the future of ICs.

*Thomas M. Frederiksen*

# Preface to the First Edition

---

Another major electronic revolution is here—the Very Large Scale Integrated (VLSI) Circuit Era. The coming changes will be more drastic than those associated with the last: The Microprocessor Revolution. These new changes will affect all of the electronic system companies, the integrated circuit (IC) designers, the IC companies, and even the system designers. In fact, the IC users of today will become the VLSI chip designers of the future.

The purpose of this book is to trace the historical evolution that has brought in the present CMOS VLSI Era. To lend perspective, Chapter 1 quickly reviews the advances that have been made in solid-state electronics and traces the evolution of both amplifying devices and logic circuits. The chapter ends with a discussion of some of the recent enhancements that have been made to the bipolar integrated circuits.

Chapter 2 traces the difficult changes that have been made in IC processes that have allowed the high volume production of Metal Oxide Semiconductor (MOS) products. This evolution is traced from the early P-channel MOS (PMOS) days, through the fast-paced, N-channel MOS (NMOS) breakthroughs, to the introduction of the early metal-gate Complementary MOS (CMOS) processes.

Chapter 3 traces the many developments that have improved the ability to fabricate complex silicon wafers. Such topics as the move from diffusion furnaces to ion implanters; the oxide isolation techniques that are both in production and are under development in research labs; the important dry etching techniques; the progress in high resolution lithography that is rapidly approaching the capability to define lines less than  $1\ \mu\text{m}$  in IC production; and the complex multi-layered IC chip interconnect schemes.

The reasons for the present emphasis on CMOS processes for the emerging VLSI Era are discussed in Chapter 4. Many aspects of this move to CMOS VLSI are considered from the standpoint of the IC suppliers, the IC customers, and the effects on the people of both groups. An interesting way to comprehend the complexities of modern ICs is provided. The approach makes use of the more familiar  $\frac{1}{4}$  inch as a scaled-up minimum resolvable dimension. Then we show the scaled-up areas that result when this scaling is applied to modern IC chips.

The wide variety of standard ICs that have been made available with the advanced CMOS processes are described in Chapter 5. These range from CMOS operational amplifiers (op amps), switched-capacitor filters and the digital-to-analog converters (DACs) and analog-to-digital (A/D) converters of linear CMOS to the many new products that are now available in digital CMOS. Changes in the telephone system that were greatly helped with CMOS products are also included.

Performance improvements of a new CMOS logic family are described and the benefits of CMOS for microprocessors and memory products are discussed. This chapter ends with a step-by-step description of a CMOS process: a multiple-layer-metal, silicon-gate wafer fabrication sequence.

Semicustom and custom circuits are discussed in Chapter 6. The popular semicustom gate arrays are described. Complete custom chips made up from standard-cell arrays, functional-block arrays, and silicon compilers are some of the IC concepts that are presented. These techniques are designed to reduce chip-design turnaround time (and cost) and place increasing emphasis on Computer-Aided Design (CAD) for VLSI. Much of the current thinking about these design possibilities and the description of the requirements for the CAD systems are presented.

The current status of the new developments in high leadcount IC packages is the subject of Chapter 7. A wide variety of both insertion-type packages and surface-mount packages are described.

Chapter 8, "A Look into the Future," discusses the many new techniques that are being considered to develop advanced single-chip VLSI systems. The importance of the new-found freedoms that exist in digital architectures are discussed and the theoretical problem of assessing an optimum architecture is mentioned. The future of silicon circuits, the Silicon Foundry, the place of software in the VLSI Era, the limits of silicon ICs, and a look at recent developments in gallium arsenide ICs are also subjects for this last chapter.

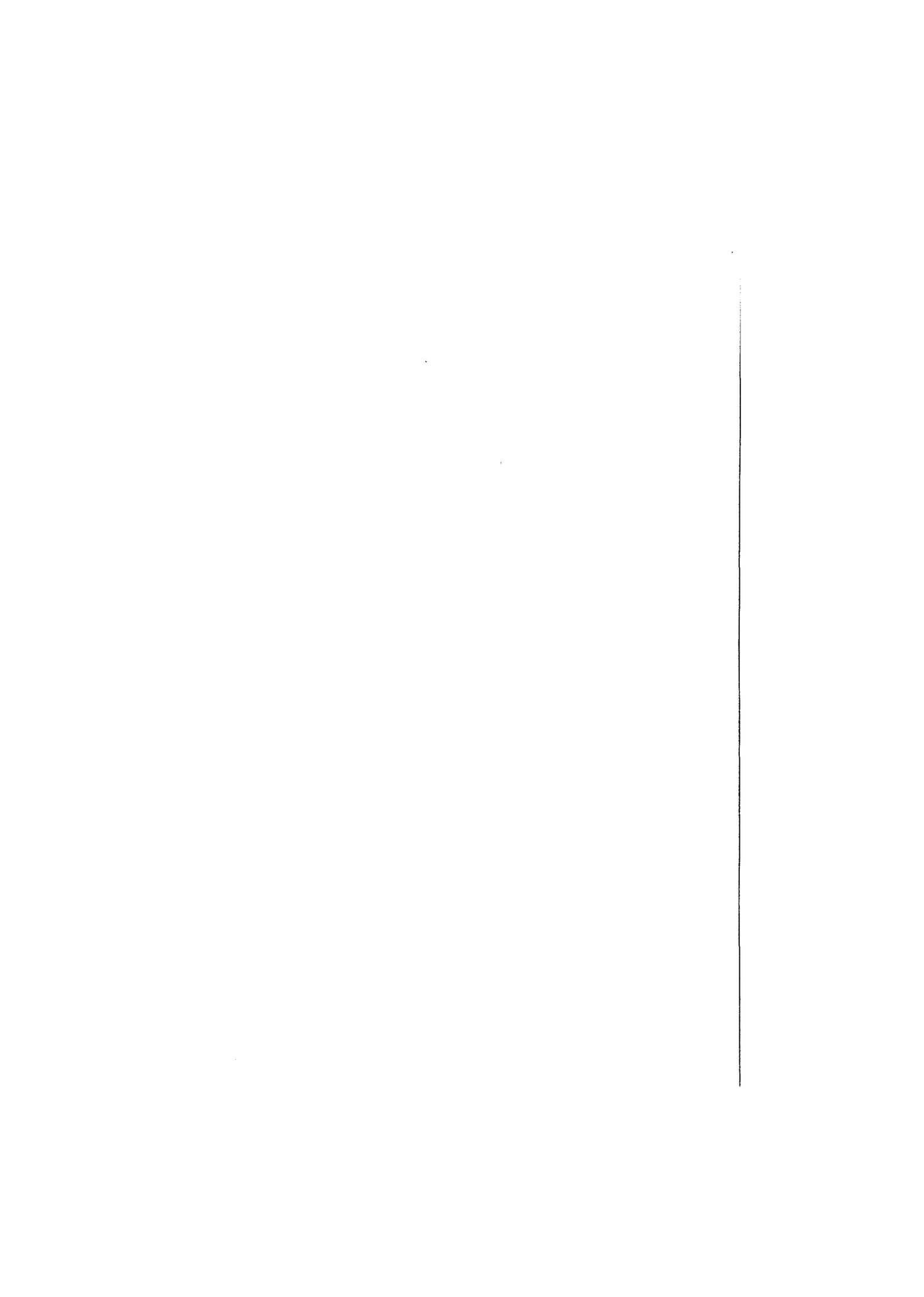
*Thomas M. Frederiksen*

# Acknowledgments

---

In trying to tell a simplified story of a very complex industry, I often found myself confused and over my head. I am very grateful to one of my best friends over the years, Bob Dort, who, during a crash course, patiently explained many of the details of the evolution in wafer fabrication. Much of this part of the story results from his perception, expertise, and long association with most of the processes and equipment used in silicon wafer fabrication.

The final manuscript also has benefitted greatly from the careful reading and comments of Matthew Buynoski, Milt Wilcox, and Mark Levi.



---

Intuitive  
CMOS  
Electronics