Analog Circuit Design

ANALOG CIRCUIT DESIGN

MOST RF Circuits, Sigma-Delta Converters and Translinear Circuits

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Preface

This book contains the revised contributions of all the speakers of the fifth AACD Workshop which was held in Lausanne on April 2-4, 1996. It was organized by Dr Vlado Valence of the EPFL University and MEAD of Lausanne. The program consisted of six tutorials per day during three days. The tutorials were presented by experts in the field. They were selected by a program committee consisting of Prof. Willy Sansen of the Katholieke Universiteit Leuven, Prof. Rudy van de Plassche of Philips Research and the University of Technology Eindhoven and Prof. Johan Huijsing of the Delft University of Technology.
The three topics mentioned above have been selected because of their importance in present days analog design. The other topics that have been discussed before are:

in 1992 :	Operational amplifiers
	Analog to digital convereters
	Analog computer aided design
in 1993 :	Mixed A/D cicuit design
	Sensor interface circuits
	Communication circuits
in 1994 :	Low-power low-voltage design
	Integrated filters
	Smart power circuits
in 1995 :	Low-noise, low-power, low-voltage design
	Mixed-mode design with CAD tools
	Voltage, current and time references

Each AACD workhop has given rise to the publication of a book by Kluwer entitled "Analog Circuit Design". This is thus the fifth book. This series of books provides a valuable overview of all analog circuit design techniques and achievements. It is a reference for whoever is engaged in this discipline. The aim of the workshop has been to brainstorm on new possiblities and future developments in the area of analog circuit design. We sincerely hope that this fifth book continues the tradition to make a valuable contribution to the insight in analog circuits in Europe and in the world.

Willy M.C.Sansen
K.U.Leuven

MOST RF CIRCUIT DESIGN

Willy Sansen

Introduction

Radio-frequency design is going through a renaissance because of the explosion of the telecommunication field. They used to be realized with discrete bipolar devices and later on in integrated bipolar technologies. Recently they have become a reality in submicron CMOS technologies as well. This first day of the AACD '96 was therefore entirely devoted to circuit design of telecommunication subsystems in CMOS technologies.

The first presentation is given by Dick Klaassen on aspects of high-frequency modelling of MOST devices. Details are given on Philips' model 9 both at DC as well as at RF frequencies up to 20 GHz. Considerable attention is paid to parasitic effects and to the behavior of elementary circuit combinations such as cascades and cascodes.

The first paper addressing the integration of full transceivers in CMOS technology is given by Paul Gray. It provides an overview of technical challenges in portable battery-powered transceivers for personal communications.

It is followed by a presentation by Patrice Senn on 2 GHz RF circuits in BICMOS technology. Extensive discussion is given on a LNA (low-noise amplifier), a mixer, a low-phase noise VCO, etc.

Michiel Steyaert then gives a presentation on the pitfals of RF CMOS design. He started with a review of the high-frequency limitations of MOST devices. This is applied to the realization of a monochip receiver, a synthesizer and a transmitter.

The fifth paper is given by Jan Sevenhans. He discusses the various implementations currently in use in commercial GSM products. He also sketches the possible merits of GaAs and future battery technologies.

Finally Asad Abidi shows several integrated circuit examples such as a digital frequency synthesizer, an upconversion mixer, an RF power amplifier, etc., all in CMOS to prove that a 900 MHz spread-spectrum wireless transceiver has become reality. Other critical problems such as an integrated inductor are discussed as well.

It can be concluded that these texts amply show that CMOS has become a viable technology for high-frequency communications applications. With the advent of more advanced submicron CMOS, even higher frequency realizations can be expected.

RF modelling of MOSFETs

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ABSTRACT

The accuracy of the Philips compact MOS model, MOS MODEL 9, has been investigated for a number of quantities, that are important for RF circuit design. On-wafer S-parameter measurements have been performed on MOS devices as a function of the frequency up to the GHz-range. From these S-parameters important RF quantities such as input impedance, transconductance, current and voltage gain etc., have been obtained. A comparison between experimental results and model calculations will be presented.

Introduction

RF circuit design in CMOS will be restricted mainly to mainstream CMOS processes. These mainstream CMOS processes are provided by foundries, which commonly supply the compact model parameters used in the circuit design. Most CMOS foundries supply parameters for rather simple compact MOS models, which are suited for digital design only. In fact there are only two public-domain compact MOS models, which are really suited for analog circuit design: the BSIM3v3 model from UC-Berkeley and the Philips compact MOS model, MOS MODEL 9 [1, 2, 3]. These models try to combine a good description of the geometry dependence of the transistor behaviour with continuous derivatives of current with respect to bias voltages.
Literature on high-frequency S-parameter measurements of MOSFETs is scarce [4]. Publications available are focused on characterization of

device and process performance (see e.g. [5] to [9]) or on test structures, measurement techniques and special effects (see e.g. [10, 11]). Measurements are compared only with calculations using special small-signal equivalent circuits. In [12] we presented the first comparison of high-frequency measurements on MOSFETs with calculations using an analog compact MOS model, i.e. MOS MODEL 9. Here we extend this comparison to a number of experimental quantities, which are important for RF circuit design.
In the following we will discuss the compact model, MOS MODEL 9, and the experimental method. Next we will present the comparison of measurements and calculations of important quantities such as input impedance, current and voltage gain as a function of frequency and bias conditions for a number of basic transistor configurations.

MOS MODEL 9

This Philips compact MOS model has been introduced within Philips in 1990 and became available in the public domain in 1993. Many of its features and capabilities have been elucidated in publications (see e.g. [12] to [18]), while the derivation of many equations and the underlying physical mechanisms are described in [19]. The complete set of equations of MOS MODEL 9 has been published in [3].
The following physical effects are taken into account by MOS MODEL 9:

- body-effect for implanted substrate;
- mobility reduction due to transversal field;
- velocity saturation;
- subthreshold region;
- drain-induced barrier-lowering;
- static feedback;
- channel length modulation;
- avalanche multiplication and substrate current.

Due to its physical basis MOS MODEL 9 (or MM9) has a minimum number of parameters per phenomenon modelled. This results in a total number of 18 parameters to model a transistor with a specific geometry. For homogeneous substrate dope the body-effect model with one k-factor is used, which implies that this number is reduced to 16. In these numbers the three parameters for the modelling of the avalanche multiplication are included. All these parameters are extracted from the dc characteristics of the transistor. Except for the oxide thickness no additional parameters are needed for the charge model. It should be noted that the charge model of MOS MODEL 9 has a bias-dependent charge partitioning between source and drain. All MOSFET capacitances are derived from this charge model.
Simple scaling rules describe the 18 electrical parameters mentioned above, as a function of channel geometry (i.e. length and width). Due to the physical basis of the model these scaling rules contain only 46 geometry-independent parameters. Additional scaling rules for the temperature dependence have also been established.

		n-channel	p-channel
Current in linear region	$V_{sb} = 0\,V$	1.2%	1.9%
	$V_{sb} \neq 0\,V$	2.8%	3.2%
Current in saturation region	$V_{sb} = 0\,V$	6.1%	4.7%
	$V_{sb} \neq 0\,V$	5.9%	5.4%
Current in subthreshold region	$V_{sb} = 0\,V$	12%	17%
	$V_{sb} \neq 0\,V$	20%	31%
Output conductance	$V_{sb} = 0\,V$	24%	15%
	$V_{sb} \neq 0\,V$	23%	16%
Substrate current		26%	27%

Table 1: Mean absolute deviation (in %) between measured and simulated (using MOS MODEL 9) characteristics averaged over several bias conditions and over 14 geometries of an 0.8 μm process (see [14]).

MOS MODEL 9 describes the transistor characteristics over the whole geometry range of a CMOS process very accurately with only one geometry-independent parameter set. This is demonstrated in Table 1,

where for the five operating regions from which the parameters are extracted, the accuracy is given (see also [14]).
As MOS MODEL 9 has been developed especially for analog applications, great care has been taken to obtain continuous derivatives of currents and charges. Consequently, MM9 complies with most benchmark tests for analog models [20, 21].

RF measurements and simulations

Small-signal scattering (S) parameters in two-port configuration have been measured with an HP8510 Network Analyzer using air coplanar high-frequency probes in ground-signal-ground configuration. Special test structures have been designed with the MOSFETs in common source-bulk configuration. For each structure also dummy structures have been designed to correct for parallel and series parasitics. The measured S-parameters have been converted to admittance (Y) parameters. The measurements on the dummy structures have been used to correct the transistor measurements for the interconnect parasitics.

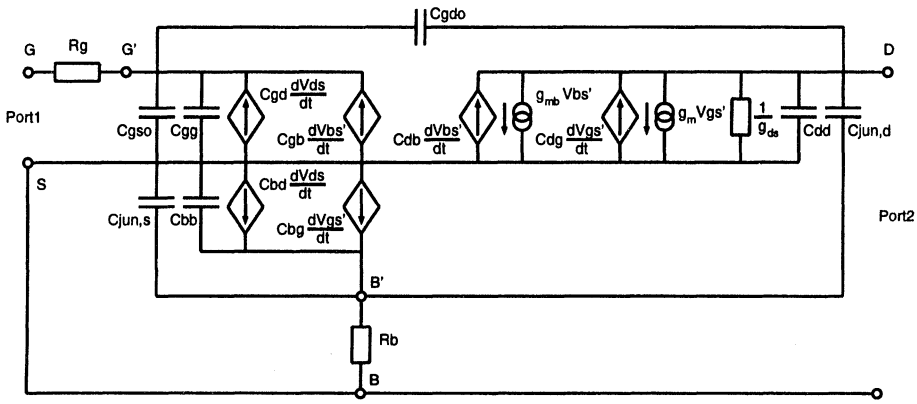


Figure 1: Equivalent circuit of MOS MODEL 9 in two-port common source-bulk configuration. The overlap capacitances, indicated with C_{gso} and C_{gdo}, are included in this model. The junction capacitances, indicated with $C_{\mathrm{jun,s}}$ and $C_{\mathrm{jun,d}}$, are described by a separate model, JUNCAP (see text). The gate resistance, indicated with R_{g}, and the bulk resistance, indicated with R_{b}, are not included in these models.

S-parameter measurements have been performed at fixed bias conditions as function of frequency as well as at fixed frequency as function of bias voltage. The overlap and depletion capacitances have been measured at low frequencies with an HP4284 LCR-meter.
For the simulations we used MOS MODEL 9 with parameters obtained from dc current measurements. The equivalent circuit in two-port common source-bulk configuration is shown in Figure 1. For the depletion capacitances the Philips model, JUNCAP, has been used [22], while the gate and bulk resistances have been added in all simulations.

Basic RF circuits

In this section we will discuss four basic RF circuits: *i*) common source-bulk configuration; *ii*) common gate configuration; *iii*) cascade configuration; and *iv*) cascode configuration. For these basic configurations a comparison will be presented of measurements and calculations of important quantities such as input impedance, current and voltage gain as a function of frequency and bias conditions.

Common source-bulk configuration

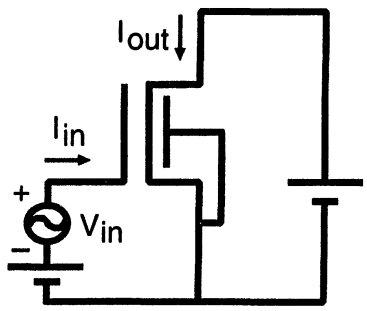


Figure 2: MOSFET in common source-bulk configuration.

In Figure 2 a MOSFET in common source-bulk configuration is shown. The gate is voltage driven, while the drain is ac short-circuited. The input impedance, $Z_{\rm in} = v_{\rm in}/i_{\rm in}$, of a MOSFET in common source-bulk configuration is shown in Figure 3 as a function of frequency. The drain bias has been chosen at 2 V, being 60% of the supply voltage of the process, while for the gate bias three values equally spaced between the threshold voltage, $V_{\rm TO} \approx 0.6\,V$, and about one Volt above $V_{\rm TO}$, have been used. For the input impedance the influence of the bulk resistance is negligible. The expression for the input impedance , $Z_{\rm in}$, yields (see Figures 2 and 1)

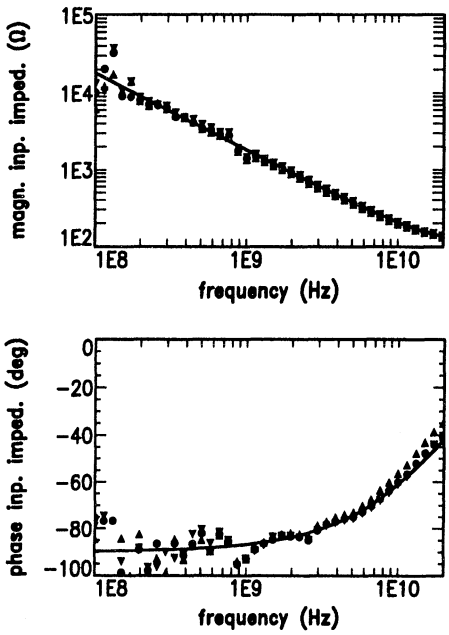


Figure 3: Magnitude (top) and phase (bottom) of the input impedance of a 60/0.5 N-channel transistor with $V_{TO} = 0.6\,V$ in common source-bulk configuration. Symbols represent measurements at $V_{ds} = 2.0\ V$ and $V_{gs} = 0.9\ V$ (downwards-directed triangles), $1.2\ V$ (solid circles) and $1.5\ V$ (upwards-directed triangles). Lines represent MOS MODEL 9 simulations. Note that the transistor has a salicidated poly-Si gate.

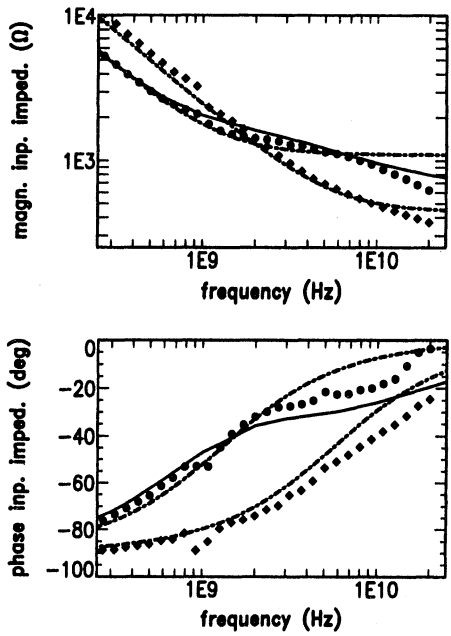


Figure 4: Magnitude (top) and phase (bottom) of the input impedance of a 40/1 (diamonds) and 100/1 (solid circles) N-channel transistor in common source-bulk configuration at $V_{ds} = V_{dd} = 5\ V$ and $V_{gs} = 2\ V$. Dashed lines represent MOS MODEL 9 simulations with one segment only, while solid lines represent MOS MODEL 9 simulations with five "distributed" parallel segments of $20\,\mu m$ wide. Note that the transistors have non-salicidated poly-Si gates.

$$Z_{\text{in}} = \frac{v_{\text{in}}}{i_{\text{in}}} \approx \frac{1}{\text{j}\,\omega\, C_{\text{gg}}^{\text{eff}}} + R_{\text{g}} \quad . \tag{1}$$

Herein $C_{\text{gg}}^{\text{eff}}$ is the effective capacitance

$$C_{\text{gg}}^{\text{eff}} = C_{\text{gg}} + C_{\text{gso}} + C_{\text{gdo}} \quad , \tag{2}$$

where C_{gso} and C_{gdo} are the gate-source and gate-drain overlap capacitances, respectively, and C_{gg} is the intrinsic capacitance

$$C_{\text{gg}} = \frac{\partial Q_{\text{g}}}{\partial V_{\text{g}}} \quad . \tag{3}$$

Here (and throughout this paper) Q_{i} is the charge of intrinsic terminal i, which is given by MOS MODEL 9 (see Figure 1).
From Figure 3 and Eq. 1 one sees that up to very high frequencies the input impedance shows a capacitive behaviour. However, for processes with non-salicidated poly-Si as gate material or transistors with a very high W/L ratio, the gate resistance may become very high. In that case the gate resistance can no longer be treated as a lumped element (see Figure 4 and Eq. 8). In Figure 5 the current gain, $i_{\text{out}} / i_{\text{in}}$, as a function of frequency is shown for the device and bias conditions from Figure 3. From this figure it is clear that MOS MODEL 9 describes both frequency and bias dependence accurately. Neglecting again the bulk resistance, one finds for the expression for the current gain (see Figures 2 and 1)

$$\frac{i_{\text{out}}}{i_{\text{in}}} \approx \frac{g_{\text{m}}}{\text{j}\,\omega\, C_{\text{gg}}^{\text{eff}}} \left(1 - \text{j}\,\omega \frac{C_{\text{dg}}^{\text{eff}}}{g_{\text{m}}} \right) \quad . \tag{4}$$

Herein g_{m} is the dc transconductance and $C_{\text{dg}}^{\text{eff}}$ is the effective capacitance

$$C_{\text{dg}}^{\text{eff}} = C_{\text{dg}} + C_{\text{gdo}} = -\frac{\partial Q_{\text{d}}}{\partial V_{\text{g}}} + C_{\text{gdo}} \quad . \tag{5}$$

For the cut-off or unity current-gain frequency, f_{T}, the familiar expression is found from Eq. 4 (see e.g. [23])

$$f_{\text{T}} \approx \frac{g_{\text{m}}}{2\,\pi\, C_{\text{gg}}^{\text{eff}}} \quad . \tag{6}$$

In Figure 6 this cut-off frequency is shown as function of gate voltage at three different drain voltages. From this figure it can be seen that MOS MODEL 9 predicts the bias dependence of f_{T} quite accurately.

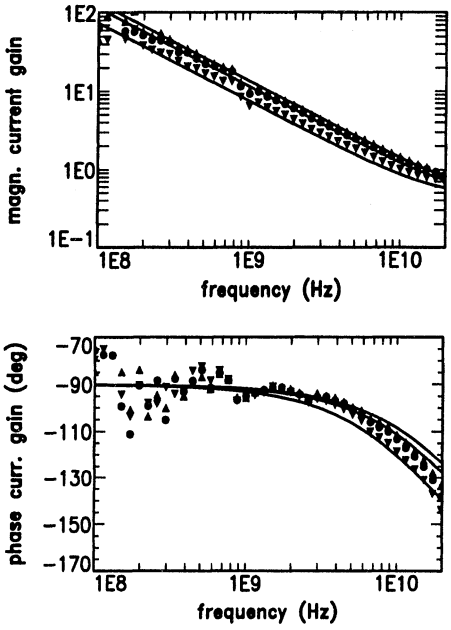


Figure 5: Magnitude (top) and phase (bottom) of the current gain of a 60/0.5 N-channel transistor ($V_{TO} = 0.6\,V$) in common source-bulk configuration. Symbols represent measurements at $V_{ds} = 2.0\ V$ and $V_{gs} = 0.9\ V$ (downwards-directed triangles), $1.2\ V$ (solid circles) and $1.5\ V$ (upwards-directed triangles). Lines represent MOS MODEL 9 simulations.

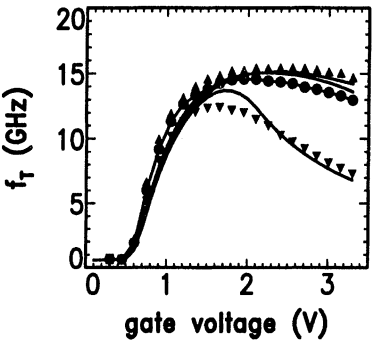


Figure 6: The f_T of a 60/0.5 N-channel transistor ($V_{TO} = 0.6\,V$) in common source-bulk configuration as function of gate voltage for drain voltages of $1\,V$ (downwards-directed triangles), $2\,V$ (solid circles) and $3.3\,V$ (upwards-directed triangles). Lines represent MOS MODEL 9 simulations.

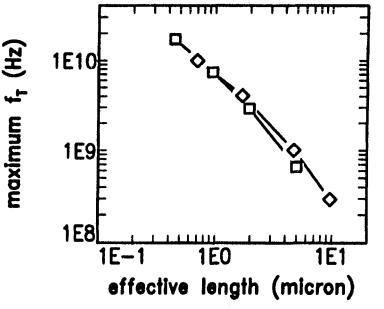


Figure 7: Measured maximum f_T as function of effective channel length. Diamonds represent N-channel devices from a $1\,\mu m$ CMOS process ($V_{dd} = 5\,V$) and squares represent N-channel devices from a $0.5\,\mu m$ CMOS process ($V_{dd} = 3.3\,V$), respectively. The measurements have been performed at $V_{ds} = V_{dd}$.

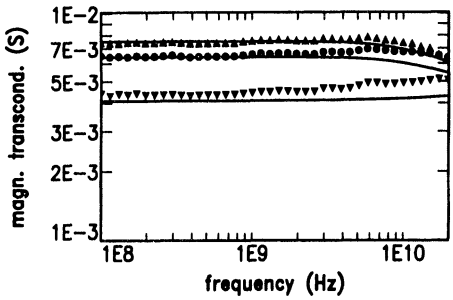
In Figure 7 the maximum f_T is shown as a function of effective gate length. From this figure it can be seen that the maximum f_T is inversely proportional to the square of the effective channel length. This implies that f_T is quite low for long-channel devices. It should be noted that due to mobility reduction for the smallest channel lengths, the length dependency of the maximum f_T is less steep.
The transconductance, i_{out}/v_{in}, of the 60/0.5 N-channel device is shown in Figure 8 as a function of frequency. From Figures 5 or 6 and Figure 8 it can be seen that below the cut-off frequency of the current gain, again the description of MOS MODEL 9 for frequency and bias dependence is quite accurate. The expression found for the transconductance is (see Figures 2 and 1)

$$\frac{i_{out}}{v_{in}} \approx \frac{g_m - \omega^2 R_g C_{dg}^{eff} C_{gg}^{eff} - j\omega\left(g_m R_g C_{gg}^{eff} + C_{dg}^{eff}\right)}{1 + \left(\omega R_g C_{gg}^{eff}\right)^2} \quad . \tag{7}$$

From Eq. 7 follows that both the real and imaginary parts of the transconductance are affected by the gate resistance. This is demonstrated in Figure 9, where the transconductance for a 40/1 N-channel transistor from a non-salicidated process is shown. From Figure 9 it is also clear that the correct expression for the resistance of a single-sided contacted gate, is (as can be shown from theory)

$$R_g = \frac{W \rho_{\square,poly}}{3L} \quad , \tag{8}$$

where $\rho_{\square,poly}$ is the sheet resistance of the poly-Si gate material. It should be noted that for a double-sided contacted gate the factor 3 in the denominator of Eq. 8 should be replaced by 12.
Once we have established the correct value of the gate resistance, it is interesting to look into non-quasi static effects, which are observed most easily from the transconductance. In Figure 10 the transconductance is shown for a number of P-channel devices with gate length varying from 0.6 μm to 30 μm. The cut-off frequency, f_T, varies between 5 GHz and 6 MHz (indicated by the arrows in Fig. 10). From Figure 10 it can be seen that for the long-channel devices both the magnitude and the phase of the transconductance show a sharp dip at frequencies above f_T. This typical non-quasi static behaviour is not described by the present quasi static implementation of MOS MODEL 9. However,



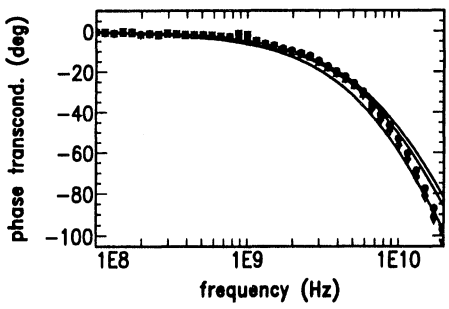
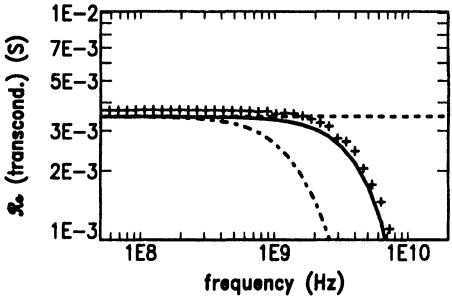


Figure 8: Magnitude (top) and phase (bottom) of the transconductance of a 60/0.5 N-channel transistor ($V_{TO} = 0.6\,V$) in common source-bulk configuration. Symbols represent measurements at $V_{ds} = 2.0\ V$ and $V_{gs} = 0.9\ V$ (downwards-directed triangles), $1.2\ V$ (solid circles) and $1.5\ V$ (upwards-directed triangles). Lines represent MOS MODEL 9 simulations.



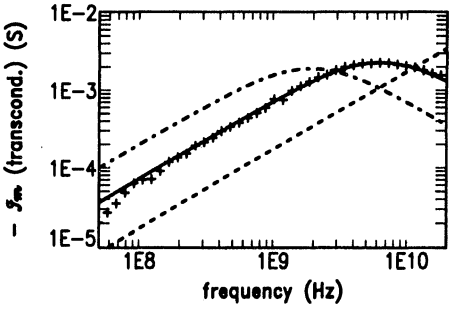


Figure 9: Real (top) and imaginary (bottom) parts of the transconductance a 40/1 N-channel transistor ($V_{dd} = 5\ V$) in common source-bulk configuration at $V_{ds} = 4\ V$ and $V_{gs} = 4\ V$. Symbols represent measurements, lines represent MOS MODEL 9 simulations with $R_g = 0$ (dashed line); $R_g = (W\rho_{\square,poly})/(3L)$ (solid line); and $R_g = (W\rho_{\square,poly})/L$ (dashed-dotted line).

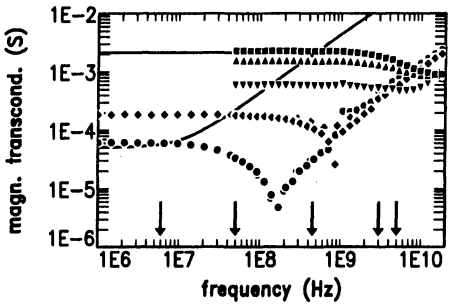


Figure 10: Magnitude (top) and phase (bottom) of the transconductance of PMOSFETs in common source-bulk configuration at $V_{ds} = 4\,V$ and $V_{gs} = 4\,V$ ($V_{dd} = 5\,V$). Gate width is 30 μm, while the gate length is 30 μm (solid circles), 10 μm (diamonds), 3 μm (downwards-directed triangles), 1 μm (upwards-directed triangles) and 0.6 μm (solid squares). Lines represent MM9 simulations for gate lengths of 30 and 0.6 μm, respectively. Arrows indicate f_T for each device.

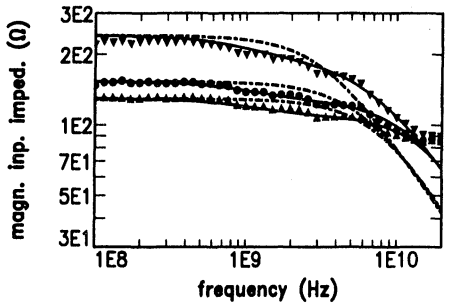


Figure 11: Magnitude (top) and phase (bottom) of the input impedance of a 60/0.5 N-channel transistor ($V_{TO} = 0.6\,V$) in common gate configuration. Symbols represent measurements at $V_{ds} = 2.0\ V$ and $V_{gs} = 0.9\ V$ (downwards-directed triangles), $1.2\ V$ (solid circles) and $1.5\ V$ (upwards-directed triangles). Dashed lines represent MOS MODEL 9 simulations without bulk resistance and solid lines represent MOS MODEL 9 simulations with bulk resistance.