In-Circuit Testing

Allen Buckroyd

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Preface

This book is written for potential purchasers and users of in-circuit automatic testers who are attracted to the concept of ICT, but who may need help. This includes Test Engineering Managers who need guidance on which equipment to buy for a given application (and how to financially justify the purchase), and ATE Programmers, Test Engineers and Technicians who would welcome practical advice on how best to use the chosen ATE.

The emphasis throughout is towards practical problem solving, and many of the examples used are of surface mount PCBs, since the trend appears to be towards this technology.

The book provides a description of what ICT can and cannot do, and answers many questions on how tests are actually carried out, with the benefits and drawbacks of the techniques. A chapter is provided on application – fitting ICT into a typical test strategy and into the manufacturing environment. The buying decision is also fully explored – choice of system, initial and ongoing costs, and preparation of the financial proposal to Management.

Then, assuming the ATE has been purchased, additional chapters are devoted to:

Programming problems and solutions
Interfacing problems and solutions
Fault diagnosis and fault finding tools.

Design for in-circuit test also merits a chapter. This covers specific design guides and the constraints which need to be placed on designers to ensure that ICT is cost effective.

The concluding chapter reviews the purchase and use of the chosen ICT with the benefit of hindsight; it covers cost effectiveness, looks at

alternative methods of testing, programming and interfacing, and alternative ways of costing the testing service. We also see the effect on yield, and the need for fault analysis, feedback to Design and to the PCB Assembly area to optimise the design and build quality.

Finally the author looks at ways of expanding ICT within the factory environment to maximise the benefits of this very worthwhile testing facility. This includes an introduction to computer integrated test, and the way integration can improve the cost effectiveness of ICT.

Abbreviations

ACI	Automatic component insertion
AEI	Automatic electrical inspection
AG2	Autoguard
AOT	Adjust on test
APG	Automatic pattern generation
AQL	Acceptable quality level
ASIC	Application specific integrated circuit
ATE	Automatic test equipment
ATPG	Automatic test pattern generator
BCD	Binary coded decimal
BIST	Built-in self test
BIT	Built-in test
BITE	Built-in test equipment
BOM	Bill of material
BUT	Board under test
CAD	Computer aided design
CAE	Computer aided engineering
CAR	Computer aided repair
CAT	Computer aided test
CIM	Computer integrated manufacturing
CIT	Computer integrated test
CNC	Computerised numerical control
DFT	Design for test
DIL	Dual in line IC
DNC	Direct numerical control
DTL	Diode transistor logic
DUT	Device under test
DVM	Digital voltmeter
EDIF	Electronic design interchange format

EDS	Engineering defining specification
EEPROM	Electrically erasable prom
EPROM	Erasable programmable read only memory
ESS	Environmental stress screening
GPIB	General purpose interface bus
IC	Integrated circuit
ICT	In-circuit test
INCITE	Instructional notation for computer controlled in-circuit test equipments
JIT	Just in time (manufacturing)
JTAG	Joint test action group
KGB	Known good board
LAN	Local area network
LSI	Large scale integration
MDA	Manufacturing defect analyser
MOS	Metal oxide silicon
MTBF	Mean time between failures
MTTR	Mean time to repair
NC	Numerical control
PCB	Printed circuit board
PPP	Program preparation package
PPS	Program preparation station
PTS	Production test specification
RAM	Random access memory
RF	Radio frequency
ROM	Read only memory
RTFA	Real time fault analysis
SA1	Stuck at one
SA0	Stuck at nought
SMD	Surface mounted device
SMT	Surface mount technology
SOT	Select on test
TAM	Test area manager
TCP/IP	Telecommunication protocol/Internet protocol
TDS	Test development services
UUT	Unit under test
VLSI	Very large scale integrated circuit
WIP	Work in progress
ZIF	Zero insertion force (connector)

1 Introduction

Let me declare my interest straight away. I am a fan of in-circuit test, or ICT for short. To a user of automatic test equipment, someone with a test problem to solve, ICT is a most valuable tool in the battle to find faults on electronic printed circuit board assemblies (PCBs). In the right circumstances, it is very cost effective, relatively easy to use, straightforward to program, and it provides the fastest way to eliminate the majority of faults on a PCB.

So what is ICT?
What does it do?
What does it not do?
How does it work?
What faults can be detected by the technique?
Can it cope with modern technology?
Who are the suppliers of equipment?

This introductory chapter provides brief answers to these basic questions, before we address the detailed aspects of the technique, the problems and the solutions.

1.1 What is ICT?

In-circuit testing covers the verification of individual components against a specification whilst actually fitted into the functional circuit board. The specification for resistance, capacitive reactance or inductive reactance takes account of and allows for the surrounding electronic environment. Figure 1.1 illustrates the principle of ICT, where A and B represent the switching matrix and interface to the BUT (board under test) which enables

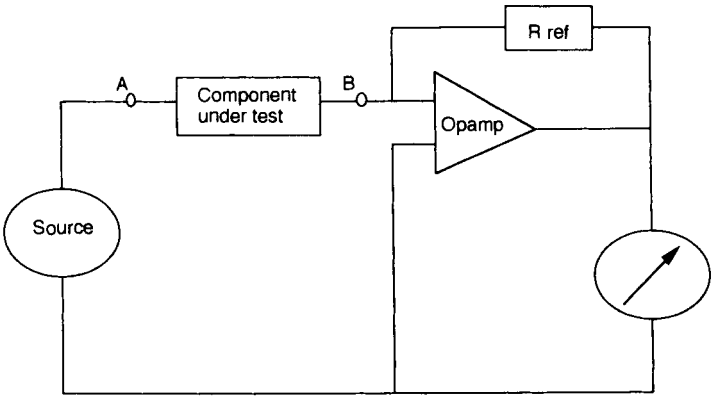

Figure 1.1 The principle of in-circuit test.

each component in turn to be connected to the measurement circuits. By suitable selection of the reference (shown as R ref, but equally valid as C ref or L ref, etc.), a very wide variety of component values can be verified, using the principle of an operational amplifier with feedback, as shown.

It is usually the first electrical test to be carried out on an assembled printed circuit board. It can stand alone as the only test performed on the PCB, but more often it forms part of a test strategy whereby it precedes several stages of functional test, resulting in a high integrity product from which the large majority of actual faults have been eliminated. Figure 1.2

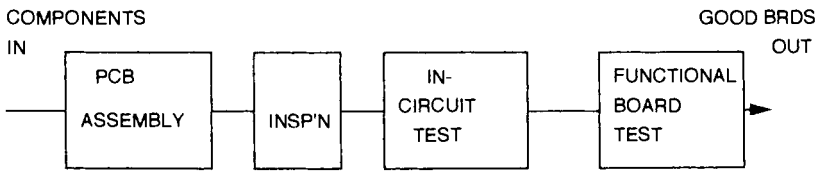

Figure 1.2 Basic test strategy.

gives a diagramatic representation of the strategy, and Figure 1.3 indicates the percentage of possible faults covered by the different test phases.

For many years the term AEI – automatic electrical inspection – was used for the operation I have just described. In its initial form, as a detector of manufacturing defects only, the term AEI was an adequate title. The equipment was often used instead of a human inspector who traditionally verified each stage of assembly by visual checks on a printed circuit board,

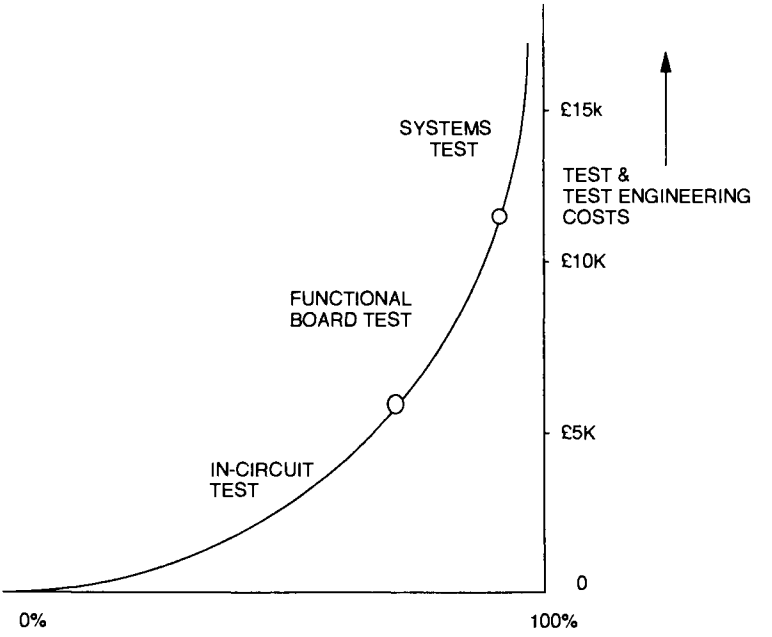

Figure 1.3 Percentage of fault cover by ICT.

and checked the processes and operators. Usually visual aids such as magnifiers and light boxes were used, but even so, many faults were missed. Nowadays, boards with smaller components and thinner track make the efficient use of manual visual inspection techniques extremely difficult.

However, the more efficient alternative to visual inspection – automatic electrical inspection – was sometimes regarded as optional, to be used or bypassed as occasion demanded, depending on time available, and on the level of assembly defects. So long as subsequent functional tests were designed to fully test the board, this stratagem was realistic. In the same way that visual inspection by humans can be carried out on 100% or a sample of PCB output, depending on the quality of the product, so too AEI could be used or skipped.

The advent of much more powerful in-circuit ATEs enabled this test stage to be made an integral part of the testing strategy, not just a pre-screen before the apparently more important functional board test (FBT). ICT became an essential first stage of PCB verification, covering areas which could not be adequately tested at functional test. For instance pull-

up resistors may be used to limit current and avoid thermal problems; their presence and correct value is much more readily checked by ICT rather than at the functional stage. Also, some logic testers are not short circuit proof, and the presence of a short may cause a drive stage in the logic ATE to be destroyed. Hence, the elimination of shorts using an ICT is essential on all boards which are intended to be tested on a digital ATE. Therefore the term "in-circuit tester" serves two purposes: it more adequately describes what these ATEs can do; secondly, by including the word "tester" in the title of the ATE, the Production Manager is prompted to realise that this ATE is a mandatory part of the test strategy for a given PCB, and he must not skip the test.

The cost effectiveness of ICT (and manufacturing defect analysis, which is a subset of it) is illustrated in Figure 1.4, a diagram commonly referred to as the Rule of Ten. Since ICT often accesses individual components directly, and is the only test strategy designed to verify the assembly process, it is capable of the most rapid diagnosis of the bulk of faults on assembled PCBs, which are catastrophic component faults and PCB assembly faults of all kinds. Diagnostic costs are therefore found to be 1/10 the cost per fault at functional board test, and 1/100 the cost per fault at functional unit stage. This provides the greatest financial argument for buying ICT ATEs.

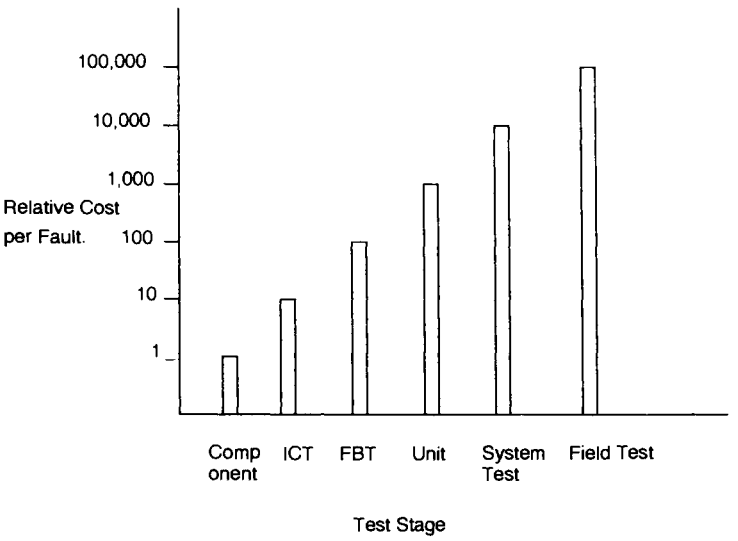

Figure 1.4 The Rule of Ten.

Different technologies will cause some variation in these cost relationships. For instance, a design containing a large number of complex integrated circuits may require a significant amount of expensive component testing prior to in-circuit PCB test, increasing the first column; a design which includes comprehensive built in test (BIT) and software diagnostics may be easier to diagnose at the system level, causing the fourth or fifth column to be reduced, but overall the relative cost advantages remain.

Note that in-circuit test is also applied to a range of field testers designed to find faults in equipment which has previously worked in the factory, but has subsequently failed in the field, that is, on the customer's premises. For logic testing these testers employ test clips connecting each integrated circuit to the tester, a different clip being required for each size or style of component. If for instance a 7474 D-type device is being accessed, the tester calls up the "truth table" for that device from the ATE database into local memory, enabling that device to then be tested " in-circuit". (Truth table testing is covered in section 1.2.2.) Analogue components can be checked using voltage and current probes, digital multimeters and special fault tracers (see Chapter 5). These testers have evolved additional features for use by field personnel with rather less detailed knowledge of the unit under test than factory trained technicians. They are intended to be general purpose, requiring the minimum of specialised programming. The method of interfacing is universal, so that dedicated interfaces are not required for each type of PCB. Some versions even employ self-learn programs. In general, however, they rely on a skilled technician using a logical approach to detect the fault, testing each device, stage by stage, until a false output is detected. The test technique takes longer than a factory-based approach, the skill level required is higher, but the ability to test in this way provides a powerful tool for field maintenance, obviating the need to hold large numbers of spare PCBs of several types, shortening the time to repair a board by cutting out the factory repair loop.

1.2 What does ICT do?

1.2.1 Three tasks

The in-circuit test technique is primarily concerned with performing 3 tasks on a newly assembled PCB:

1) Proving the processes of PCB assembly;
2) Eliminating straightforward component faults as soon as possible in the testing phase;
3) Satisfying such parts of the test verification strategy which are best covered on an ICT ATE.

This is achieved by checking each component, or group of components ''in circuit'' or ''in situ''. For example, if a resistor forming part of a circuit is electrically tested by probing the circuit nodes to which it is fitted, and making various measurements, we can satisfy ourselves on the following points:

- that the resistance value is within a prescribed tolerance,
- that the circuit nodes are connected to the resistor (since a result of say 100 MΩ will indicate a non-connection, an open circuit),
- that the resistor is not illegally connected to earth or V_{cc} (usually +5 V), or to any other non-valid circuit node (this covers short circuit faults).

Hence passive measurements can be made on resistors, capacitors, inductors and transformers, checking their nominal value. Diodes and transistors can be checked to verify their correct position in the circuit; diodes can have their forward and reverse functionality checked and transistors tested to verify that they can be switched on and off. Such tests of course only partially check these devices.

1.2.2 Logic testing

A logic device will receive additional tests on those ICT ATEs which have a logic test capability. A library of ''truth table'' tests for each of the many hundreds of proprietary devices is held within the memory of the ATE. When the test program reaches a given logic device, the appropriate truth table is applied to the inputs, i.e. a sequence of 1s and 0s is called up, and applied to the input pins in a given order. The actual responses of the gate under test are compared with known good answers held as part of this truth table, within the ATE. Such a pattern, suitable for a ''NAND-gate'' with 2 inputs and 1 output is given in section 1.4.4 below.

This test is not normally performed at high speed, but at a rate of a few thousand tests per second, which is often referred to as a slow algebra test. Specialist logic tester ATEs are capable of testing at millions of tests per

second. However, if the logic content of the board is small, logic testing within the in-circuit test stage is very cost effective, and will find the majority of catastrophic logic faults in small and medium scale logic devices. An extension of the individual truth table testing is functional block testing where combinations of logic devices are checked overall to determine their conformance to a limited truth table test. This is a useful feature which can significantly reduce the test time in specific circumstances by testing only the actual logic function being carried out, rather than the sum of all the logical functions of all the chips.

1.2.3 Two, four and six wire measurements

The ATE also contains a switching matrix to enable any pair of pins to be accessed by the measuring circuits, and to enable the circuit to be stimulated. Four wire and six wire measurements are also common features on many machines, designed to eliminate the errors in measurement which can be made when the circuit being tested carries significant current. The voltage drop in the circuit caused by the product of the current and stray impedance is thereby overcome.

Briefly, the four wire technique allows two wires to feed the component with suitable current stimulus, accepting that there will be a voltage drop along these two wires. A second pair of wires are used to monitor the voltage directly across the component under test, and the wires are fed to a high impedance circuit which draws negligible current, Hence the voltage measured within the ATE represents the true voltage across the component (see Figure 1.5).

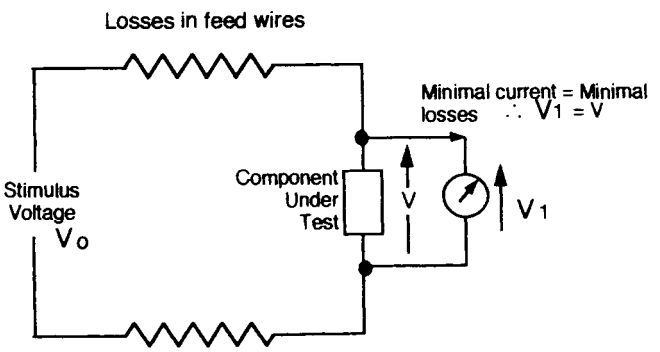

Figure 1.5 Four wire measurement.

Six wire measurement is an extension of the same idea, wires 5 and 6 being used for special guarding. Guarding describes the technique used to minimise the effect of parallel components in the area of measurement.

1.2.4 Track integrity tests

''Track integrity'' is a specific term to describe the verification of the copper track, to establish that separate tracks really are separate, with no copper or solder short circuit connections, neither to earth, V_{cc} nor to other tracks. It could also be used to establish that a piece of track (also called a land or a net) is continuous from end to end, with no breaks or high resistance points. To perform this test would require probes on the ends of all tracks. As this may require very large numbers of probes, even on a moderately complex PCB, it is not usually carried out directly on assembled boards. A decision on an open circuit can often be drawn when very high readings are given by the ATE when measuring component values. An open circuit soldered joint is much more likely than an internal open circuit in a resistor, say, and components which are open circuit through damage should be easy to detect visually. Detection of open circuit track is best carried out at the bare board test stage; probes are connected to each component land area (not just one per net as in ICT fixtures), enabling the fault to be pin-pointed to a small area of the PCB in most cases.

1.3 What does ICT not do?

1.3.1 Functional testing

ICT is *not* designed to check the functionality of the PCB, hence this is normally outside the scope of most testers on all but the simplest electronic circuits. However, it can be assumed that if the circuit has been properly designed, that no track faults exist, that all component tests pass, the likelihood is that the circuit will function, though not necessarily to its full specification. Functional board test (FBT) is often the next test after ICT, applying parametric analogue stimulus or digital patterns to check the functionality of the board to its specification. Plate 1.1 shows this in action.

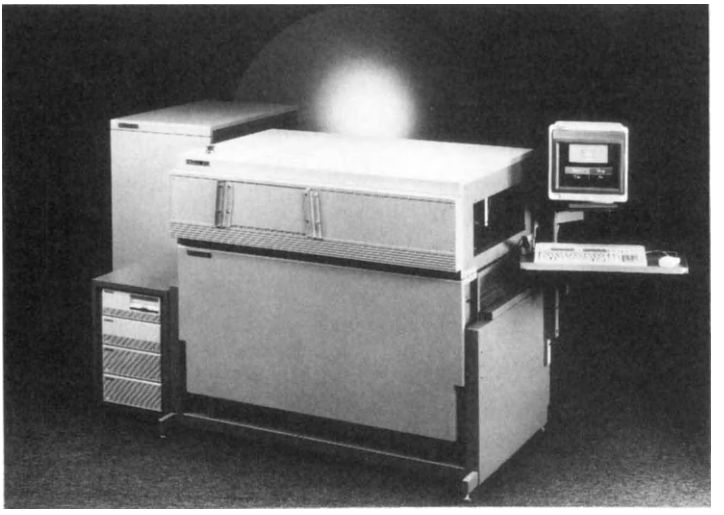

Plate 1.1 HP 3070 SMT series combinational ATE (photo courtesy of Hewlett-Packard).

1.3.2 Complex VLSI test

ICT is *not* designed to test complex integrated circuits. Special testers are made for this purpose, and if VLSI (very large scale integration) devices are purchased against well thought out specifications, and normal precautions are taken against static and physical damage during handling, assembly and test, then the likelihood of VLSI related faults at the PCB test stage will be small (compared to say process faults). However, VLSI is becoming more complex, and more common, with a million gates/transistors or more inside a chip one inch square. Unfortunately, perfection is not guaranteed by the VLSI suppliers. Hence some thought must be given to:

- possible failure mechanisms which can cause obscure faults which may occur at system stage or in use,
- the wisdom of built in self test (BIST) features designed into the silicon to aid device, PCB and system testing,
- boundary scan circuitry built into silicon to verify that the VLSI is properly connected into the circuit (i.e. that soldered joints are good and that IC plug and socket connections are sound).

1.3.3 High accuracy testing

ICT will *not* make high accuracy measurements of circuit parameters. This is due to two main factors:

- stray capacitance due to wires between the probes and the measurement circuits,
- use of close tolerance rather than very high tolerance components in the measurement circuitry in the ATE, mainly to keep the price competitive.

Hence normal ICT ATEs are capable of measuring to within say ±3% of the actual value of the component. When setting limits during programming, this percentage is added to the tolerance of the component under test, i.e. to measure 10 kΩ ±5% the machine looks for 10 kΩ ±8%. This is not a significant disadvantage in practice on most circuits. Most resistance faults are not, in my experience, marginal. Resistors tend to be either within tolerance or well outside tolerance, possibly open circuit internally or broken; operators have been known to fit 1 kΩ instead of 10 kΩ (or vice versa). However, for precision circuits using very close tolerance components ICT may not be precise enough to verify the value of passive components, and additional functional tests will be required to prove the circuit.

1.3.4 Full speed testing

ICT does *not* test circuits at their working speed. Since components are checked individually, in sequence, finite time must be allowed for the switching operation, for capacitors to charge before measuring their impedance, and for logic to settle. In some ATEs reed relays are used for switching; these are slower than logic switches but of lower resistance. There may be a trade-off between speed and accuracy. It could be argued that all digital testing should be at full clock rate. I have personally detected "slow" components in the past, but these were DTL (diode/transistor logic) devices. We used to "tune" the select on test collector loads to achieve minimum switching time between sequential logic stages (an operation which took many days during computer system test in the 60s). With the advent of TTL (transistor/transistor logic) the problem of slow devices largely disappeared.

Moreover, ICT was never designed or intended to be a full speed logic tester (though it must be said that test speeds have continuously increased year after year). It is designed to seek out faults such as the wrong device fitted, or device fitted incorrectly. In this context testing at 50 MHz say is unnecessary.

1.3.5 Parametric testing

In-circuit test does *not* deal with parametric measurements of gain, frequency, noise, etc. Such tests are "functional", implying an extension of the fundamental ICT concept. Combinational ATEs have been designed to combine in-circuit with functional test in one machine (see Plate 1.1). This use of one framework or box plus one combined interface may result in lower overall test equipment capital costs, and may permit faster turn-round of PCBs through the combined ICT + functional test, especially if automatic mechanical handling is also included. However, the capacity of the ATE in terms of PCBs tested per hour is likely to be less than with 2 or more separate ATEs. Hence the use of combinational ATEs must be carefully worked out to avoid wastage of ATE facilities, hence inefficient usage. This is dealt with again in Chapter 2 on ICT application.

Hence in-circuit test must be used for the purposes for which it is best suited – the rapid identification of straightforward faults. When used for other, less appropriate tasks, the cost effectiveness of the technique suffers. In practice this could mean a large increase in programming and interfacing for each extra (non-appropriate) task, or a large increase in run time for such a test, at the expense of throughput on straightforward tests.

1.4 How does ICT work?

The basic technique involves accessing circuit nodes on the board via a bed-of-nails interface, and programming the ATE to measure component values " in-circuit", one at a time.

1.4.1 Interfacing

The method of connection to the circuit under test involves accessing all or most of the circuit nodes on the assembled board via a "bed-of-nails " (BON) interface. The nodes are physically represented by the soldered leads of the components on a conventional leaded assembly, or by special

test pads connected by copper track to component terminations on a surface mounted PCB (see Figure 1.6). The contact to the nodes themselves is by the "nails" or spring loaded probes in the interface, which are wired back to driver and receiver circuits inside the ATE.

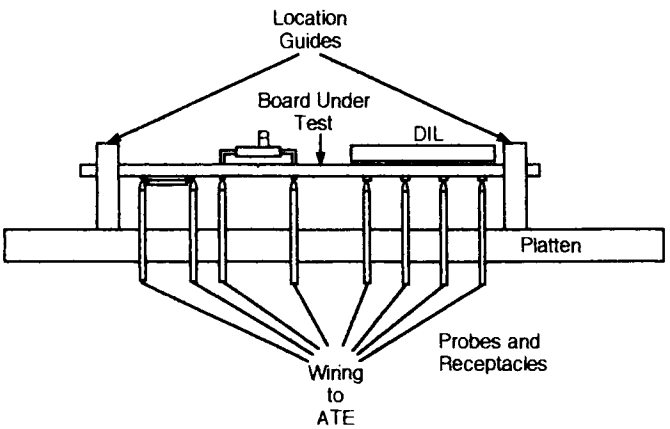

Figure 1.6 ICT interface.

For the sake of clarity I have omitted various mechanical details, only the location guide being shown. This ensures accurate registration between the board under test (BUT) and the ICT probes. It involves drilling tooling holes of approximately 2–3 mm diameter near the corners of the blank board during the NC drilling stage. In the relaxed state the BUT is clear of the probes, being held in position by springs in the interface. The closure of the board onto the probes is done by one of three methods on the majority of ICT machines:

- mechanically via a lever,
- pneumatically via pistons,
- by vacuum pull-down, using atmospheric pressure and a vacuum pump.

Each method has advantages and disadvantages and is appropriate for different circumstances. These points will be expanded later in Chapter 4.

1.4.2 Programming

Programming for ICT involves inputting the component data for each component or test, with appropriate tolerances. This is usually done in a particular sequence, depending on the ATE. For instance, one could test all resistors, capacitors and inductors, starting with low values and progressing to high values. This is preferable to progressing numerically through the item list or bill of material, the reason being that within the ATE different measurement circuits are required to be switched into use for different ranges of components; different frequencies are used to maintain accuracy in the calculation of

$$X_L = 2.\pi.f.L$$

$$X_C = 1 / 2.\pi.f.C$$

where X is reactance in ohms, f is frequency in hertz, L is inductance in henries, C is capacitance in farads, $\pi = 2.417$.

1.4.3 Test sequence

The objective is to make an accurate check as easily and quickly as possible. Hence repeated switching from one range to another and back again should be avoided, by organising the ordering of tests. Initial checks of the track are performed using very low voltages, so that a short circuit of the power rail to earth for instance does not result in damage to the PCB, by a copper track burning out. Such faults will cause the test sequence to halt, allowing the fault to be eliminated before passing on to the next stage. For the same basic reason the on-board voltage sources are measured before power-on tests are initiated. This covers the possibility of voltage rails being out of specification. TTL logic rails have a tolerance of ±0.25 V, hence if the nominal +5 V rail is badly regulated, or is faulty, and results in +5.25 V or more, all the TTL logic devices on the board could be damaged. Even if they appeared to be working when tested, it might be judged that their reliability had been impaired, and they should all be replaced. Changing perhaps a hundred 14 or 16 pin devices is quite likely to damage the board itself, rendering it unsaleable. Hence the need for great care in devising the test sequence.

1.4.4 Node forcing

Back driving or node forcing is a term describing the means by which logic testing is carried out on an individual logic device in-circuit. In a passive state, some logical outputs will be held in a low or a high state. However, to test the inputs of the following gate with both logical 0 and 1 inputs, it will be necessary to override the previous outputs, forcing the nodes into a high current state. This "forcing" is limited in duration by the ATE to avoid overdriving the outputs and damaging devices. It has been proved by ATE suppliers, and accepted by equipment users, that so long as the pulse ON/OFF ratio is limited to 1:500 with a maximum duration in the forced state of 1 ms, and a high forcing voltage of not more than 3 V peak (including overshoots), and source and sink current limited within the test system to 0.5 A maximum, all will be well. However, customers such as British Telecom have stated that they expect PCB suppliers to be able to demonstrate the integrity of their test methods and systems, and to replace components which can be shown to have been damaged by node forcing. It is advisable therefore that users of node forcing use device models (which determine factors such as ON/OFF ratio) from the ATE supplier, rather than devise their own models. This limits the liability for damage, since ATE suppliers who supply the facility for node forcing will have of necessity limited the tendency to overdrive. I know of no component suppliers who actually *recommend* node forcing, though they recognise that the technique exists. They test chips individually, so have no need to use back driving. Here follows an explanation of the node forcing technique and problems, using Figure 1.7.

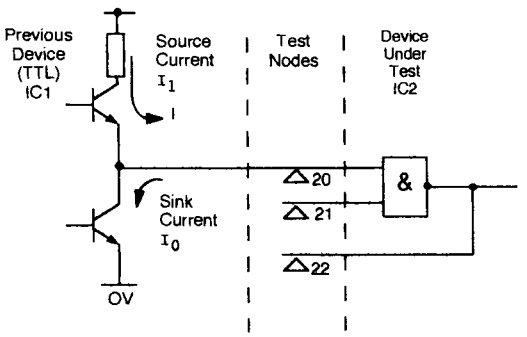

Figure 1.7 Principle of node forcing.